Time-Dependent Dielectric Breakdown in High-Voltage GaN MIS-HEMTs: The Role of Temperature

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***Abstract*— We have investigated time-dependent dielectric breakdown in high-voltage AlGaN/GaN metal–insulator–semiconductor high-electron mobility transistors, with a focus specifically on the role of temperature under positive gate stress conditions. We aim toward understanding the temperature dependence of progressive breakdown (PBD) as well as hard breakdown. We find that the temperature dependence of time-to-first breakdown, hard breakdown, and the gate current evolution during PBD all share similar, shallow activation energies that suggest a common underlying mechanism. However, the gate current noise during PBD seems to be independent of temperature and is likely due to a tunneling process. Understanding of temperature-dependent breakdown is essential to developing accurate device lifetime estimates.**

***Index Terms*— Dielectric reliability, GaN, metal–insulator–semiconductor high-electron mobility transistor (MIS-HEMT), progressive breakdown (PBD), temperature dependence, time-dependent dielectric breakdown (TDDB).**

I. Introduction

As THE demand for energy-efficient power electronics increases, GaN has emerged as a promising candidate for high-voltage power management applications. The AlGaN/GaN metal–insulator–semiconductor high-electron mobility transistor (MIS-HEMT) constitutes the most promising device structure as it offers low gate leakage current and high channel conductivity. GaN has excellent material properties, but there are still many challenges to overcome before widespread commercial deployment is possible [1]–[3]. Time-dependent dielectric breakdown (TDDB), a catastrophic condition arising after prolonged high-voltage gate stress [4], is a particularly important concern. Thus far, studies under positive gate bias stress have shown TDDB behavior similar to that of silicon CMOS systems [5]–[9].

In this paper, we explore the temperature dependence of positive gate stress TDDB in order to deepen our physical understanding of TDDB in the GaN MIS-HEMT system. Though depletion-mode GaN devices are typically operated in a cascode configuration for safety [10], [11], the OFF-state condition in the cascode yields a peak in the electric field at the drain-side edge of the gate [2] that complicates the electrostatics and is undesirable for a fundamental understanding of TDDB in GaN. TDDB under the OFF-state stress condition has been recently explored elsewhere [12]. Depletion-mode devices are not designed to operate above a gate bias of 0 V, but positive gate stress yields a relatively uniform electric field underneath the gate and makes a fundamental study of TDDB simpler and more insightful.

Though the statistical failure distributions are well understood, what is missing is work that begins to explore the specific nature of the defects that underlie TDDB in GaN MIS-HEMTs. Temperature-dependent studies can help provide this insight. They also allow us to explore the linkages between the different device degradation modes that appear before catastrophic final breakdown. Furthermore, a thorough knowledge of the temperature acceleration of TDDB is necessary for accurate device lifetime estimation. There have been few studies on TDDB and the role of temperature in GaN MIS-HEMTs to date [5], [13], [14]. This paper expands on an unpublished conference presentation [15].

II. Experimental Initial Results and Statistics

The devices studied in this work are industrially prototyped depletion-mode AlGaN/GaN MIS-HEMTs with a SiN gate dielectric, and a gate area of 2000 μm^2 fabricated on 6-in Si wafers. They feature three field plates placed in a stairway fashion along the gate-to-drain gap resulting in a breakdown voltage $>$600 V. All experiments were carried out using an Agilent B1505A power device analyzer and a cascade tesla probe station.

Transistors were stressed under positive gate voltage, $V_{GS,stress} > 0$ V, while keeping $V_{DS,stress} = 0$ V. This induces

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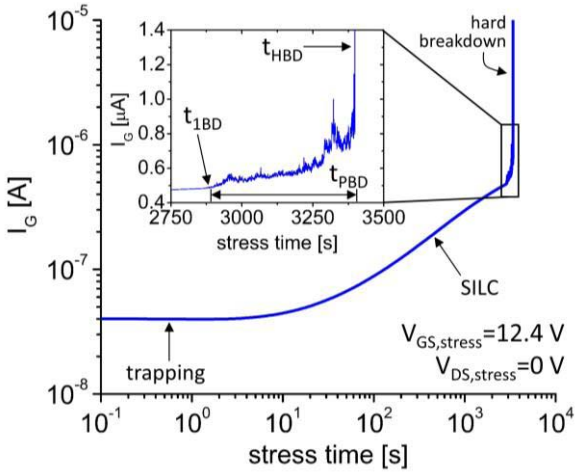

Fig. 1. Gate current I_G as a function of stress time during a constant $V_{GS,stress}$ TDDB experiment at RT. The MIS-HEMT is held at $V_{GS,stress}$ = 12.4 V until the device breaks down. $V_{DS,stress}$ = 0 V. The inset shows a clear onset of noise in I_G marking the beginning of the PBD regime.

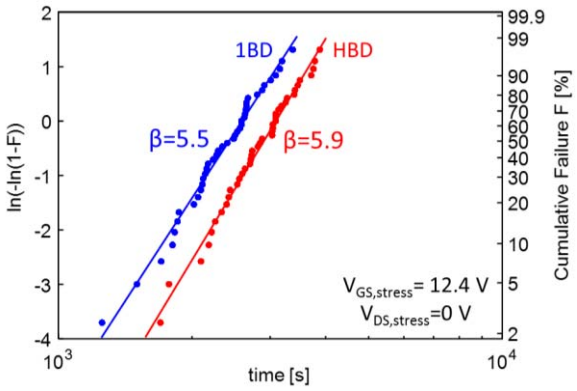

Fig. 2. Weibull plot of t_{1BD} and t_{HBD}. $V_{GS,stress}$ = 12.4 V and $V_{DS,stress}$ = 0 V at RT. Nearly parallel statistics for time-to-first breakdown 1BD and HBD suggest a unified degradation mechanism.

a high-density 2DEG at the AlGaN/GaN interface below the gate. During electrical stress, the bias gate current was continuously monitored. In an earlier study, we found that prolonged positive gate stress in these devices yields a breakdown behavior consistent with TDDB [6]. We also found evidence of progressive breakdown (PBD) prior to final hard breakdown [7].

Fig. 1 shows the evolution of the bias gate current I_G in a typical constant-voltage TDDB experiment at $V_{GS,stress}$ = 12.4 V at room temperature (RT). The slight decrease of I_G in the initial stages of the experiment is indicative of trapping [16], and the increase of I_G thereafter can be attributed to stress-induced leakage current (SILC) [17]. Dielectric hard, i.e., catastrophic, breakdown (HBD) is observed to take place around 3400 s. The inset shows that approaching HBD, I_G becomes noisy, a condition known as PBD [18]–[20]. This is distinct from the SILC that is observed earlier. While SILC is the increased leakage that results from defects being generated at random inside the dielectric [21], PBD reflects the formation of a breakdown path created by these defects within the dielectric [22]. After the onset of PBD, further stress increases the I_G noise until HBD occurs. We denote the time at which the gate noise appears as the time-to-first breakdown t_{1BD} the time at which final hard breakdown occurs as t_{HBD}, and the time lapse in between as the length of PBD or t_{PBD}.

Fig. 2 shows a Weibull plot for time-to-first-breakdown t_{1BD} and time to HBD t_{HBD} of 40 devices stressed under identical conditions. Well-behaved Weibull statistics are observed. The two data sets exhibit steep Weibull slopes [23] β of 5.5 and 5.9 for 1BD and HBD, respectively, suggesting that we are observing intrinsic breakdown.

The nearly parallel shift in the Weibull distributions of 1BD and HBD hints at a common origin for the two phenomena. The application of gate stress beyond t_{1BD} continues to generate defects at random inside the dielectric. Eventually, HBD occurs when enough energy is suddenly delivered to a dominant breakdown path that it causes it to become nearly ohmic [24].

These initial experiments establish a preliminary understanding of first breakdown and hard breakdown that suggest the two are linked. In order to further our understanding, we turn to the use of temperature next.

III. Understanding the Role of Temperature

TDDB in silicon CMOS systems is well known to have a negative temperature dependence [25], [26] at a constant stress voltage; as the temperature increases, time-to-breakdown decreases. The activation energy is also reported to vary with electric field [25], [27], [28] and for the Si MOS system, these reports range from about 0.4–1.3 eV for SiO_2. The choice of dielectric also plays a role in the activation energy, as reports of activation energies in SiN MIM capacitors are quite different from those of SiO_2 [16], [29], [30] and high-k dielectrics [31], [32]. There have been very few studies on the temperature dependence of TDDB in the GaN MIS-HEMT system and only reports of an activation energy of 0.24 eV could be found [5], [13].

In order to study the temperature dependence in our GaN MIS-HEMT system, we select four different temperatures and carry out a set of constant-voltage TDDB experiments at each temperature. We choose temperatures of 150 °C, 75 °C, 25 °C, and −25 °C and at each temperature we stress ten identical devices. All devices tested were from the same die; the devices tested at any one temperature were interspersed throughout the available devices so as to remove any systematic differences due to location on the die. All experiments follow the protocol described in the previous section.

Fig. 3 shows the gate leakage evolution for the four sets of TDDB experiments at a $V_{GS,stress}$ = 13 V. We observe that I_G leakage increases with increasing temperature. We can also see that for each temperature, the gate leakage evolution for all ten devices is nearly identical. This suggests a very uniform device fabrication process consistent with the steep β observed in the breakdown statistics of Fig. 2. There is also clear evidence of SILC at each temperature as evidenced by the increase in gate leakage current with stress time. Approaching hard breakdown, there is also clear evidence of PBD in all devices.

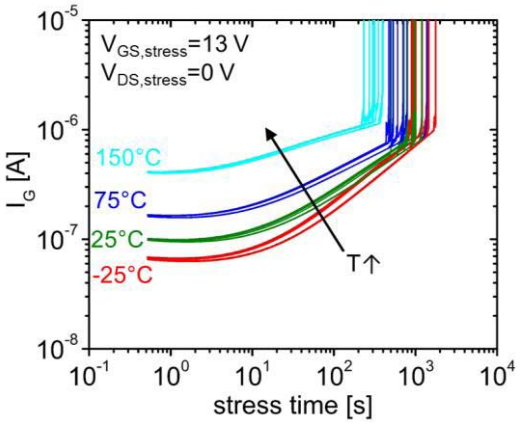

Fig. 3. Gate current I_G as a function of stress time during a series of constant $V_{GS,stress}$ experiments for different temperatures (ten devices at each temperature). The FETs are held at $V_{GS,stress} = 13$ V until the gate dielectric breaks down. As the stress temperature increases, I_G increases as well. PBD is visible near the end of the TDDB experiments.

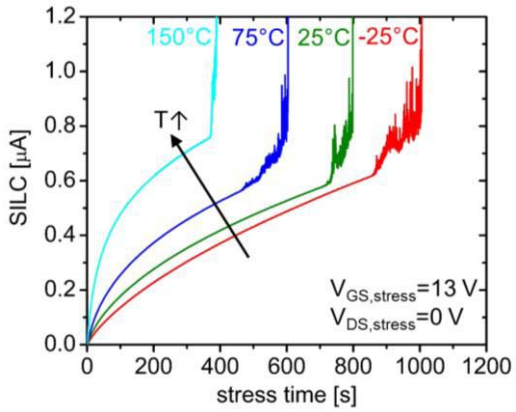

Fig. 4. SILC as a function of stress time for a representative device at each temperature during a series of constant $V_{GS,stress}$ experiments. The FETs are held at $V_{GS,stress} = 13$ V until the gate dielectric breaks down. As the stress temperature increases, the rate of increase of SILC increases as well. This is consistent with faster rates of defect generation at higher temperatures.

Given the slopes of each line in Fig. 3, it may seem that the rate of defect generation decreases with increasing temperature (slopes of I_G evolution get smaller with higher temperature). This would suggest that SILC generation slows down with increasing temperature, something inconsistent with the shorter breakdown times at higher temperature that are observed. Fig. 4 shows the SILC extracted from the overall gate current I_G using the methodology in [17] for a representative device at each selected temperature. This approach removes the impact of trapping that occurs most significantly for short time scales during the TDDB experiment and which is also influenced by temperature. We can now observe that the slope of SILC (rate of defect generation) increases with increasing temperature—a picture consistent with the shorter breakdown times for high temperature.

Fig. 5 shows the Weibull statistics for the TDDB experiments in Fig. 3. As expected, both t_{1BD} [Fig. 5(a)] and

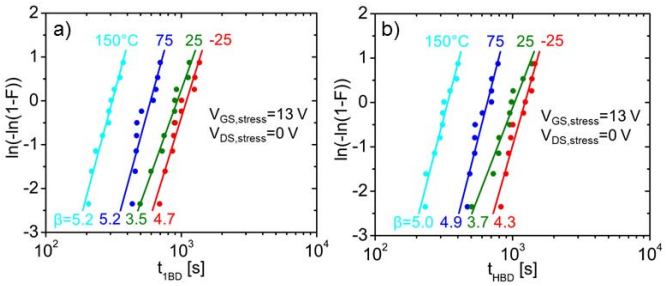

Fig. 5. Weibull plots of (a) t_{1BD} and (b) t_{HBD} at four different temperatures: 150 °C, 75 °C, 25 °C, and −25 °C. $V_{GS,stress} = 13$ V and $V_{DS,stress} = 0$ V. As the temperature increases, time-to-breakdown decreases. The slope of each set of breakdown statistics β is shown at the bottom of each graph.

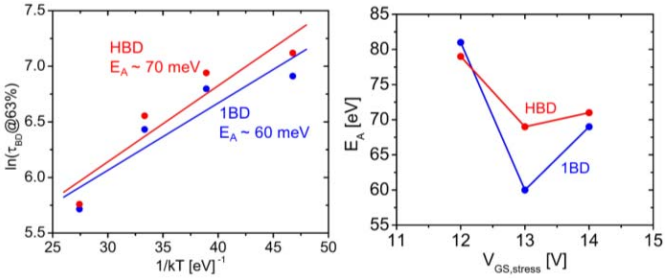

Fig. 6. (left) Arrhenius plot of t_{1BD} and t_{HBD} from Fig. 4. τ_{BD} is extracted at a cumulative device failure of $F = 63.2\%$ for every temperature. Lines drawn as guides for the eye. E_A for both 1BD and HBD are very similar, suggesting a common underlying physical mechanism. (right) Activation energy as a function of $V_{GS,stress}$ for both 1BD (blue line) and HBD (red line). No definitive trend is shown across the three values of $V_{GS,stress}$ tested and E_A remains small in each case.

t_{HBD} [Fig. 5(b)] decreases with increasing temperature. There is some variation in the observed β slope for each set of statistics, which can be attributed to the relatively small number of samples available for study [33].

To extract the activation energies for both t_{1BD} and t_{HBD}, we must pick a representative time τ_{BD} for each of the four temperatures. While sometimes a cumulative failure of 50% is chosen, a more common approach is to choose the x-intercept where the Weibull term equals zero. This corresponds to a cumulative failure of 63.2% and yields better accuracy [33]. Following this approach, we extract the activation energy [34] for first breakdown and hard breakdown by taking the linear fit to the data in the Arrhenius plot of Fig. 6(left). We find activation energies in the range of 60–70 meV for both 1BD and HBD, suggesting that the two share a common physical origin. These activation energies are also significantly smaller than reports in silicon as well as other GaN MIS-HEMT systems [5], [25], [35]. However, they are consistent with other reports of activation energy for this particular gate dielectric [29], [30], [36].

It is well-known that in the silicon CMOS system, the measured activation energy depends on the applied gate bias [25]–[27], [37]. Fig. 6(right) shows the extracted activation energies E_A for the three different $V_{GS,stress}$ values measured. Fig. 7 shows the first breakdown and hard breakdown statistics for two other values of $V_{GS,stress}$ 14 and 12 V.

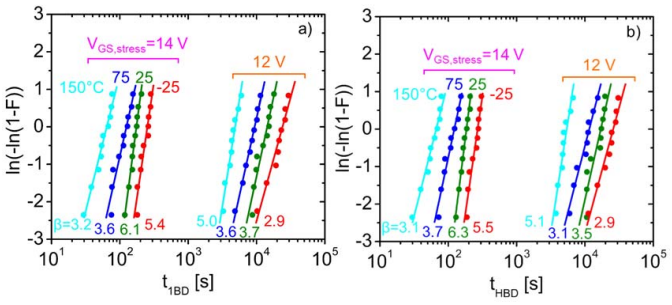

Fig. 7. Weibull plots of t_{1BD} and t_{HBD} at four different temperatures: 150 °C, 75 °C, 25 °C, and −25 °C , and at two different $V_{GS,stress}$: 12 and 14 V. (a) and (b) show t_{1BD} and t_{HBD}, respectively. As the temperature increases, time-to-breakdown decreases. As $V_{GS,stress}$ decreases, time-to-breakdown increases. The slope of each set of breakdown statistics β is shown at the bottom of each graph. $V_{DS,stress} = 0$ V in all cases.

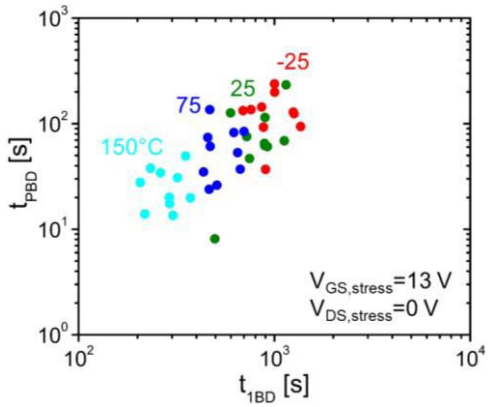

Fig. 8. PBD time versus time-to-first-breakdown t_{1BD} for all 40 samples in Fig. 3 stressed at $V_{GS,stress} = 13$ V and $V_{DS,stress} = 0$ V at different temperatures. The data show that t_{1BD} and t_{PBD} are uncorrelated. As temperature increases both t_{1BD} and t_{PBD} decreases.

We observe that in all cases, the activation energies are very small. Also, there is some variation in E_A with T, with a higher E_A for $V_{GS,stress} = 12$ V. However, this is likely due to the small statistical sample size. There is not nearly as definitive of a trend as was observed with silicon devices [27].

Parallel statistics and similar activation energies might suggest that 1BD and HBD are deterministically linked in every individual device. That is actually not the case. Fig. 8 shows t_{1BD} plotted against its corresponding PBD time [38], t_{PBD} for all 40 samples at $V_{GS,stress} = 13$ V. No correlation is observed. Once first breakdown occurs, additional gate stress continues to generate defects at random. Eventually, hard breakdown takes place when enough energy is suddenly delivered to a dominant breakdown path so that it becomes nearly ohmic [24]. Thus, from device to device, we expect the time-to-first breakdown and the time to hard breakdown to be uncorrelated but the overall statistics to be similar. That is what is observed in Fig. 8 where random distributions are obtained at all temperatures. Because t_{PBD} is the measure of time between hard breakdown and first breakdown, the fact that t_{PBD} is uncorrelated with t_{1BD} suggests that first breakdown and hard breakdown are independent of one another.

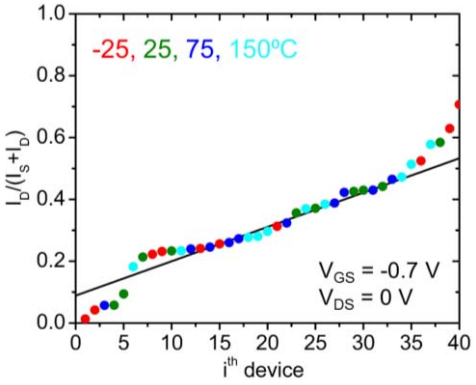

Fig. 9. Cumulative distribution plot of the ratio $I_D/(I_S + I_D)$ after HBD. V_{GS} = -0.7 V and V_{DS} = 0 V for 40 devices measured in this study. Measurements at RT. At all stress temperatures, the distribution appears random. A fit to the distribution is shown by the black line. The longer gate-to-drain distance results in a higher drain resistance estimated as $R_{Daccess} = 5 * R_{Saccess}$, from the black line. This causes the current ratio to skew more toward the source.

Fig. 9 shows a plot of the ratio $I_D/(I_S+I_D)$ after hard breakdown for all 40 devices stressed at $V_{GS,stress} = 13$ V, measured at $V_{GS} = -0.7$ V at RT. The ratio of the drain current to the total drain and source current (i.e., gate current) is indicative of the hard breakdown location laterally in the channel [39]. The results of Fig. 9 show an expected random spread of hard breakdown locations laterally along the channel at all temperatures. The spread of breakdown locations reinforces the hypothesis of random defect generation throughout the gate dielectric. The preferential weighting toward the source in our devices is not unreasonable because in this device design, the gate-to-drain access region is longer than that of the gate-to-source and so $R_{Daccess} > R_{Saccess}$. In fact, we find a reasonable fit for the data for $R_{Daccess} = 5^* R_{Saccess}$.

Our temperature-dependent studies strongly reinforce the preliminary findings that first breakdown and hard breakdown share a common physical origin, but are brought about by a random process of defect generation in the dielectric [7].

IV. Progressive Breakdown and Temperature

Having focused primarily on hard breakdown and first breakdown, we can now turn our attention to the regime in between the two: PBD. The evolution of the gate current during the PBD regime, as well as the origin of the noise, is still a topic of discussion [22], [40], [41]. We can once again leverage our temperature-dependent data in an effort to further our knowledge.

It has been observed in silicon MOSFETs [34] that the evolution of the average of the gate leakage current after first breakdown follows an exponential law in time. In fact, we can fit our PBD data for each temperature with an equation of the form $I_{G1}*\exp([t-t_{1BD}]/\tau_{PBD})$, where I_{G1} is the gate leakage current at first breakdown and τ_{PBD} is a characteristic time constant for the exponential PBD growth (i.e., the inverse slope of the straight line that results from a log-linear (I_G–t_{1BD}) plot, as in Fig. 10). The exponential growth with time and a fit is shown for different temperatures in Fig. 10 (one device per temperature). Because t_{1BD} increases with temperature,

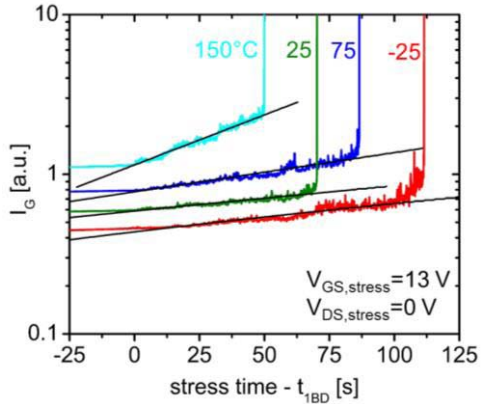

Fig. 10. Gate current I_G evolution for a typical constant-voltage TDDB experiment at each temperature: 150 °C, 75 °C, 25 °C, and −25 °C . x-axis is shown as stress time—t_{1BD} so that 1BD begins at 0 s. I_G data at different temperatures have been shifted to AUs) such that I_G evolution at each temperature is separable and visible. Also shown is an exponential fit for the PBD regime, fit to the form $I^*_{G1}\exp([t-t_{1BD}]/\tau_{PBD})$, where I_G is the gate current at first breakdown, and t_{1BD} is the time at which 1BD occurs.

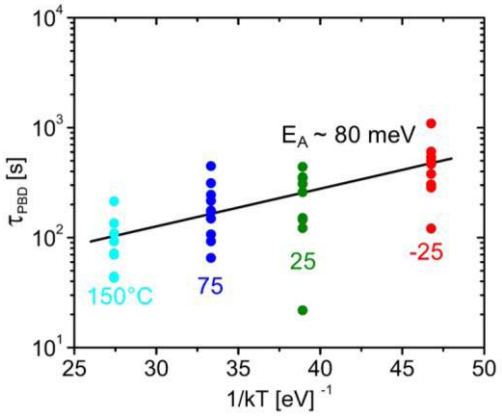

Fig. 11. Characteristic PBD growth time constant τ_{PBD} as a function of temperature. PBD growth time was fit with an exponential as shown in Fig. 10. τ_{PBD} increases as the temperature decreases, with an activation energy $E_A \sim 80$ meV.

the x-axis has been shifted by t_{1BD} at every temperature such that the onset of noise begins at 0 s. I_G data at different temperatures have been shifted to arbitrary units (AUs) so that the I_G evolution at each temperature is visible. We do indeed see exponential growth, and it is clear that the rate of growth increases with increasing temperature.

The extracted τ_{PBD} for all devices at every temperature is graphed in Fig. 11 in an Arrhenius plot. We see that τ_{PBD} decreases with increasing temperature; that is, the higher the temperature, the faster I_G ramps up after first breakdown. We can estimate the activation energy of τ_{PBD} by taking the average of τ_{PBD} at every temperature (ten devices per temperature). We find an activation energy of ∼80 meV. This value is close enough to the E_A for first breakdown and hard breakdown that it is likely all three have an origin in the same degradation mechanism responsible for the rate of formation of breakdown paths inside the dielectric.

The final piece we can explore is the appearance of noise on the gate current during PBD. It is thought that the root cause

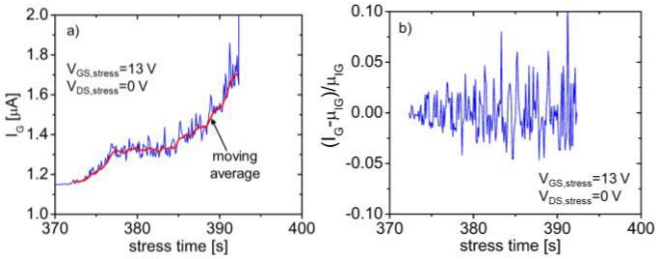

Fig. 12. PBD noise analysis illustrated for a breakdown experiment at T = 150 °C. (a) Moving average μ_{IG} of the gate current is obtained during PBD. This gives the background gate leakage current during PBD, μ_B. (b) Average I_G is subtracted from the gate current, leaving only the noise component. The data are then normalized by the average gate current to account for differences in background leakage at different temperatures (Fig. 3).

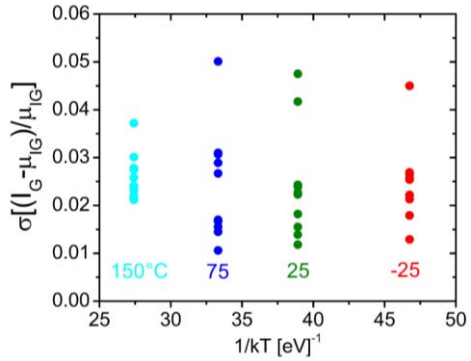

Fig. 13. Standard deviation of the normalized noise on the gate current I_G during PBD. No real trend is observed as a function of temperature, suggesting that the underlying mechanism for the PBD noise may be a tunneling phenomenon.

of this noise is trapping and de-trapping processes occurring in the breakdown conduction path [42]. Our TDDB data across various temperatures should allow us to determine if this trapping and de-trapping process relies on tunneling or is a thermally activated mechanism.

To examine the noise during PBD, we take the approach shown in Fig. 12. In order to isolate the noise from the background gate leakage current, we obtain a moving average of the gate current μ_{IG} as depicted as the red line in Fig. 12(a). We then subtract the average current from the instantaneous I_G, and this leaves us with the noise component. However, since the background gate leakage is also a function of temperature, as can be seen in Fig. 3, we also normalize the noise by this average background current and obtain the final result of Fig. 12(b). We obtain a picture that is consistent with what is seen in Fig. 12(a), that is, as the stress time increases, the noise level of the gate current increases as well.

We can then estimate the overall magnitude of the noise by taking the standard deviation of Fig. 12(b) and comparing these values across temperature. Fig. 13 shows an Arrhenius plot of the result. We observe no clear trend as a function of temperature. From this, it seems reasonable to conclude that the noise arises from electron tunneling in and out of defects along the breakdown path and the conducting characteristics of this path are not affected by temperature. The nature of these detects is yet unknown and merits further study.

V. Conclusion

Our experimentation reveals a rich picture of dielectric breakdown in the GaN MIS-HEMT system. The statistical behavior is consistent with that seen in Si devices, and the parallel distributions for time-to-first-breakdown 1BD and time to hard breakdown HBD strongly suggest the two have the same physical origin. This is reinforced by the similar activation energies that can be extracted from the temperature-dependent experiments. We do, however, find that though these breakdown modes have the same origin, they are not linked in an individual device and they are driven by the same random process of defect generation that underlies the entire TDDB process. The physical nature of these defects has not yet been determined and should be explored in further detail.

The evolution of the gate current during the PBD regime additionally provides evidence to suggest that the increase in the gate leakage current is also linked to the same defect generation underlying hard breakdown and first breakdown. First breakdown, hard breakdown, and this gate current evolution (represented by the PBD growth time constant τ_{PBD}) all have similar, shallow activation energies. The shallow activation energy of all these processes represents a marked difference with Si, however, and could suggest a different mode of defect generation.

We lastly see that the gate current noise during PBD shows no trend with temperature. If, as it is believed, the origins of noise is in electron trapping and de-trapping in the dielectric, the absence of a temperature dependence points to a tunneling process.

These measurements deepen our physical understanding of the TDDB phenomenon in the GaN MIS-HEMT system. This understanding is critical in order to develop an accurate, robust lifetime model.

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